ECE 313 Computer Organization
Syllabus
Spring 2012

Catalog Description
The features of a digital computer are examined at various levels. Topics include: CPU architecture and instruction sets (machine level), the microprogramming level, virtual memory (operating system level), the assembly language level. Prerequisite: ECE 211

Course Description
Digital computer systems have revolutionized technology and society. Fueled by exponential improvements in integrated circuit technology and considerable human ingenuity, computer systems have evolved over the last 50 years from vacuum-tube behemoths that occupied entire buildings to small chips that are used virtually everywhere. This course explores the organization and implementation of modern computer systems. Specific topics include computer system performance, instruction set architecture, integer and floating point arithmetic, the interaction between software and hardware, processor implementation, memory systems, input/output, and multiprocessor/multicore computer systems. Concepts will be reinforced with projects using the Verilog Hardware Description Language (HDL).

Instructor
Dr. John A. Nestor
AEC 426
610.330.5411 (office)
908.203.8766 (home)
nestorj@lafayette.edu
Office Hours: T R 10:30AM - 12PM or by appointment

Class Meetings
Class Meets: M W F 2:10-3:00PM, 429 AEC

If class is cancelled due to weather, I will email the class and leave a recording on my voicemail.

Attendance at all lectures is required; excessive absences will reduce your final grade. If for some reason you cannot be present for an exam, you must notify me ahead of time in order to arrange a makeup.

Textbook

Hard copies of PowerPoint slides (distributed in class).

Course Website
All course material will be posted on the Lafayette Moodle course management system (http://moodle.lafayette.edu - log in using your network ID) The posted material includes:

- Lectures
- Homework solutions
- Old Exams
- Support materials for projects (i.e., Verilog files)
**Academic Honesty**

All students are expected to adhere to the Student Code of Conduct as described in the Lafayette College Student Handbook:

“To maintain the scholarly standards of the College and, equally important, the personal ethical standards of our students, it is essential that written assignments be a student’s own work, just as is expected in examinations and class participation. A student who commits academic dishonesty is subject to a range of penalties, including suspension or expulsion. Finally, the underlying principle is one of intellectual honesty. If a person is to have the self-respect and the respect of others, all work must be his/ her own.”

**Grading**

<table>
<thead>
<tr>
<th>Component</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two 50-Minute Exams (Tent. Dates: W 2/29, W 4/11)</td>
<td>40%</td>
</tr>
<tr>
<td>Final Exam (comprehensive)</td>
<td>25%</td>
</tr>
<tr>
<td>Projects</td>
<td>25%</td>
</tr>
<tr>
<td>Homework</td>
<td>10%</td>
</tr>
</tbody>
</table>

Following ECE Department policy, a take-home **Entry Exam** will be administered during the first week of class to assess your proficiency in prerequisite material. It will not be counted as part of your course grade, but must be completed.

**Homework Policy**

The goal of the homework assignments in this course will be to reinforce your learning without penalizing you for making early mistakes. Ideally, you will then avoid these mistakes on exam problems. Problems will be marked for correctness but will be given partial credit for a good faith effort as long your work is reasonably neat and legible. Homework solutions will be made available on Moodle after each assignment is collected.

You are welcome to ask me about homework problems, and you should feel free to work with other students on problems – but please don’t waste your time by outright copying another student's solutions or solutions you found on the web.

**Projects**

In this course, you will learn about several different digital hardware structures which are the foundations of Computer Systems. To reinforce your understanding of these structures, you will complete a series of Design Projects using the Verilog Hardware Description Language (HDL). In each project, you will be given a Verilog “working model” of a structure that can be simulated to demonstrate the details of its operation. You will then extend this structure to add new features and simulate it to demonstrate that these features work correctly. These projects will also improve your skills in HDL-based design, which is the design method of choice for most modern digital systems. You will use these skills next Fall in the ECE 491 Senior Project and may also find that they are in demand in jobs that involve digital design.

Projects will be individual unless specifically noted in the assignment. Sharing project code constitutes Academic Dishonesty (see above).

**Course Topics (Tentative)**

- **Week 1 (Jan. 23-27)**
  1. Course Overview
  2. Performance Basics

- **Week 2 (Jan. 30- Feb. 3)**
  3. Technology Trends
  4. Advanced Performance
  5. Instruction Sets
Week 3 (Feb. 6-10)
   6. Instruction Sets: MIPS
   7. Instruction Sets: Software Concerns I

Week 4 (Feb. 13-17)
   8. Instruction Sets: Software Concerns II
   9. Integer Arithmetic and Logic
  10. Multiplication and Division

Week 5 (Feb. 20-24)
   11. Verilog Modeling and Simulation I (Project 1)

Week 6 (Feb. 27 - Mar. 2)
   12. Floating Point Arithmetic
      Exam 1 – Wed. Feb. 29 (Tentative)

Week 7 (Mar. 5-9)

Week 8 (Mar. 12-16)
   Spring Break – No Class

Week 9 (Mar. 19-23)
   14. Verilog Modeling and Simulation II
   15. Verilog Single-Cycle Processor Design (Project 2)

Week 10 (Mar. 26-30)
   16. Processor Design – Multi-Cycle Approach
   17. Pipelined Processor Design I

Week 11 (Apr. 2-6)
   18. Pipelined Processor Design II
   19. Advanced Pipelined Processor Design

Week 12 (Apr. 9-13)
   20. Verilog Pipelined Processor Design (Project 3)
      Exam 2 – Wed. Apr. 11 (Tentative)

Week 13 (Apr. 16-20)
   21. Memory Hierarchy I
   22. Memory Hierarchy II

Week 14 (Apr. 23-27)
   23. Memory Hierarchy III
   24. Virtual Memory

Week 15 (Apr. 30 – May 4)
   25. Storage and I/O
   26. Multiprocessors and Multicore Systems

Note: this schedule is tentative. See the Moodle page for the most up-to-date schedule.
Learning Outcomes

Upon completion of this course, students should be able to:

1. Describe the high-level organization of a computer system in terms of its major components.

2. Use performance metrics and perform basic performance calculations using the "Performance Equation" described in the text.

3. Describe how instructions are represented in memory and the operation of the processor fetch/execute cycle.

4. Describe the characteristics of different instruction sets, and be able to read and write short assembly-language programs in a specific architecture (MIPS).

5. Describe how computer systems represent different data types (i.e. integer, floating point, characters, etc.) , and be able to convert between these representations.

6. Design arithmetic circuits including adders, subtractors, ALUs, multipliers, and dividers.

7. Describe the general process used to create a processor design from an instruction set specification.

8. Design, modify, and analyze processor implementations using the single-cycle and pipelined implementation schemes.

9. Describe the basic technologies used in modern memory systems (e.g., dynamic RAM, static RAM) and their impact on processor design and performance.

10. Describe the concept of a memory hierarchy, including cache, main memory, and virtual memory.

11. Describe the different approaches used for implementing processor I/O subsystems.

12. Describe the basic organization and operation of multiprocessor and multicore computer systems.

Privacy Statement

Moodle contains student information that is protected by the Family Educational Right to Privacy Act (FERPA). Disclosure to unauthorized parties violates federal privacy laws. Courses using Moodle will make student information visible to other students in this class. Please remember that this information is protected by these federal privacy laws and must not be shared with anyone outside the class. Questions can be referred to the Registrar's Office.

Prepared by John Nestor